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Substitute for form 1449A/PTO	**Complete if Known**	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*	Application Number	10/017,669
	Filing Date	October 30, 2001
	First Named Inventor	Youfeng Wu
	Group Art Unit	2122
	Examiner Name	Unassigned
Sheet	1	of	2	Attorney Docket Number	42390P10350

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.¹	U.S. Patent Document Number	Kind Code² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
(init)	A	5,999,736		Gupta et al.	12-07-1999	
(init)	B	6,044,221		Gupta et al.	03-28-2000	

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.¹	Foreign Patent Document Office³	Number⁴	Kind Code⁵ (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T⁶

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				Attorney Docket Number	42390P10350

OTHER ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
✓	C.	PATH PROFILE GUIDED PARTIAL DEAD CODE ELIMINATION USING PREDICATION, by RAJIV GUPTA, et al., PACT "97, November 11-15, 1997 in San Francisco, California	
	D.	COMPILER-DIRECTED DYNAMIC COMPUTATION REUSE: RATIONALE AN INITIAL RESULTS, by DANIEL A. CONNORS, et al., Department of Electrical and Computer Engineering Center for Reliable And High-Performance Computing, University of Illinois, Urbana, IL 61801, Nov. 1999	
	E.	IMPROVING TRACE CACHE EFFECTIVENESS WITH BRANCH PROMOTION AND TRACE PACKING, by SANJAY JERAM PATEL, et al., Advanced Computer Architecture Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, Michigan 48109-2122	
	F.	THE SUPERBLOCK: AN EFFECTIVE TECHNIQUE FOR VLIW AND SUPERSCALAR COMPILATION, by WEN-MEI W. HWU, et al., Center for Reliable and High-Performance Computing, University of Illinois, Urbana-Champaign, Illinois, 61801.	
✓	G.	REPLAY: A HARDWARE FRAMEWORK FOR DYNAMIC PROGRAM OPTIMIZATION, by SANJAY J. PATEL, et al., Center for Reliable and High-Perfomance Computing, The University of Illinois at Urbana-Champaign, CRHC Technical Report # CRHC-99-16, December 1999	

Examiner Signature	*Hozengun Antonyogueyen Ba*	Date Considered	9/3/04

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